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QUARTERLY TECHNICAL REPORT #3
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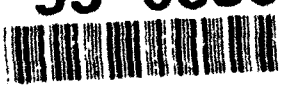


1.0 Emitter Fabrication

1.1 Mask Design and Procurement

1.1.1 Mask Set #1

As reported previously, mask set #1 was designed and procured in the first quarter and used in the processing of an L16 Taguchi experiment in the second quarter. The same mask set was used in a follow-up experiment in the third quarter. The significant findings from the first mask set that influenced the design of the second mask set were as follows:

1) The original size of a chip was based on experience with semiconductor devices and was too small to dice adequately on the silver substrates.

2) The one micron emitter tips were too small and had fully open gate apertures on only a few samples. As a result, the relative number of one micron pyramids should be much less than 1.5, 2.0 and 2.5 μm pyramids. The three larger sizes were, in general, properly formed on all samples.

3) As a result of the large number of arrays on each chip, only a small fraction could be bonded to the header. Furthermore, the bonding pad arrangement made it difficult to run bond wires in certain directions without the wires crossing over an emitter array.

4) Scribe streets were located too near the bond pads and may have resulted in some emitter to gate short circuits.

5) Dimensional stability of the silver substrates caused some missalignment of the gate metal to the emitter tips resulting in emitters on the edge of an array not being properly formed.

None of the mask difficulties was fatal and we developed work-around strategies for each of the problems.

1.1.2 Mask Set #1

As a result of the observations made from the first mask set we compiled a new set of design rules for mask set #2. The new design rules address each of the above shortcomings:

1) The new mask was designed around a set of larger chips (2x2 mm). These chips are designed to fit precisely on TO5 headers and in general have about 8 devices that can be bonded. The bond pads are located at the edge of the chip to minimize the bond length and eliminate cross over.

2) Scribe streets were made larger and located a minimum 0.1mm from the nearest bond pad to prevent bond pad shorts to the emitter plane.

3) Only a small number of arrays with 1μm tips were included. Many large arrays of 10,000 tips or more were included.

4) Gate metal patterns are desinged to completely cover the tip arrays even in the presence of some degree of misalignment. This should prevent edge effects in the emitter arrays.

The second mask set was designed and ordered in December with the first layers expected to be delivered in late January.

1.2 Process Optimization Experiments

1.2.1 Process #1.1

The first experiment consisting of an L16 orthogonal array to study 4 critical process parameters was completed in the third quarter. Initial problems with the design rule caused samples 1-8 to be rendered useless to study electrical parameters (although physical parameters were extensively studied). The experiment was therefore reduced to samples 9-16 which consisted of only two metals (Pt and Au). The experiment, nevertheless, resulted in some important findings that were helpful in the design of the second experiment. First of all, we discovered that the etch planarization step had little or no effect on the tip geometry. We made this finding from the first eight samples and essentially eliminated this variable from samples 9-16. Secondly, a major contribution to the leakage current of the device was cleaning step in the procedure. In fact this cleaning step masked any difference in leakage currents resulting from the different dielectrics (SiO_2 and Si_3N_4) or the thicknesses of these dielectrics. This change was made on samples after #12. In addition we attempted to rinse these salts believed to be responsible for surface leakage by immersing chips from sample #12 for several days in deionized water without success.

The following general observations were made on the physical characteristics of the samples from the first experiment:

1) Aperture diameters ranged from 3000 Å to about 2.0 μm.

2) Smallest apertures were obtained on the smallest pyramids and thus the pyramid tip tended to be well below the plane of the aperture.

3) Some large pyramids with large apertures had tips above the plane of the aperture.

4) There were no glaring trends relating emission current to geometry for the space of geometries studied in this experiment.

5) There seemed to be much more variation from sample to sample than there was on any particular sample. That is despite the fact that on a single header there were three devices with often very different geometries, their emission characteristics were not drastically different.

6) There was some scaling observed in emission current between the largest arrays (10,000 and 20,000 tips) and the "standard" arrays of 400 tips.

7) The choice of tip metal between Au and Pt did not have any apparent effect on the emission characteristics.

Please refer to the testing section for a more detailed discussion of the realationships between geometry and emission current.

1.2.2 Process #1.2

We developed a new technique to obtain thick dielectric without compromising the submicron apertures of the FEA in an off-line trial. The feasability study was so successful that we decided to implement the technique in experiment 1.2. Experiment 1.2 consists of 8 samples with the characteristics shown in table I below.

Sample	Dielectric Thk.	Tip Coating
17	0.83 µm	Au
18	0.83 µm	Au
19	0.83 µm	Mo
20	0.83 µm	Mo
21	0.97 µm	Mo
22	0.97 µm	Mo
23	0.97 µm	Au
24	0.97 µm	Au

Prior to this experiment we had some difficulty in obtaining a dielectric thickness greater than 0.5µm without compromising the aperture size in our gate metal. For the first time, in these experiments, we will have small apertures with emitter tips at various levels relative to the aperture. The first of these samples will be tested in January.

2.0 EMITTER TESTING

2.3 I-V TESTING

A large number of samples have been measured. Testing has yielded mixed results and a full analysis of the device performance with respect to their fabrication parameters is still underway. In table I we show a summary of the testing that has been accomplished to date with only brief performance indications. Those devices that failed hard (i.e. shorted) are denoted with a failed status. The results shown in the various figures in this section are the best performance results obtained. Some samples show unambiguous and reasonable emission. Most samples have relatively high leakage between the emitter and the gate. This high gate leakage ultimately seems to be the causes of the device failure.

The measurement vacuum system can accommodate up to 16 devices. Each device is measured sequentially with a circuit consisting primarily of three Keithely source measurement units. Each current in the circuit (i.e. the emission current, the gate current and the anode current) are measured independently by a separate Keithely source measurement units. The test plan is to run a survey scan of all of the devices that are loaded into the vacuum system for a run. The survey scan limits the leakage current to 0.1 micro-amperes. If a device shows some emission further runs are made on that device. All of the devices are processed up without much aging, due primarily to the volume of samples. In figure 1 a device that exhibited a high emission current relative to the leakage current is shown. Figure 1 clearly shows that the current in the anode follows almost identically the current from the emitter.

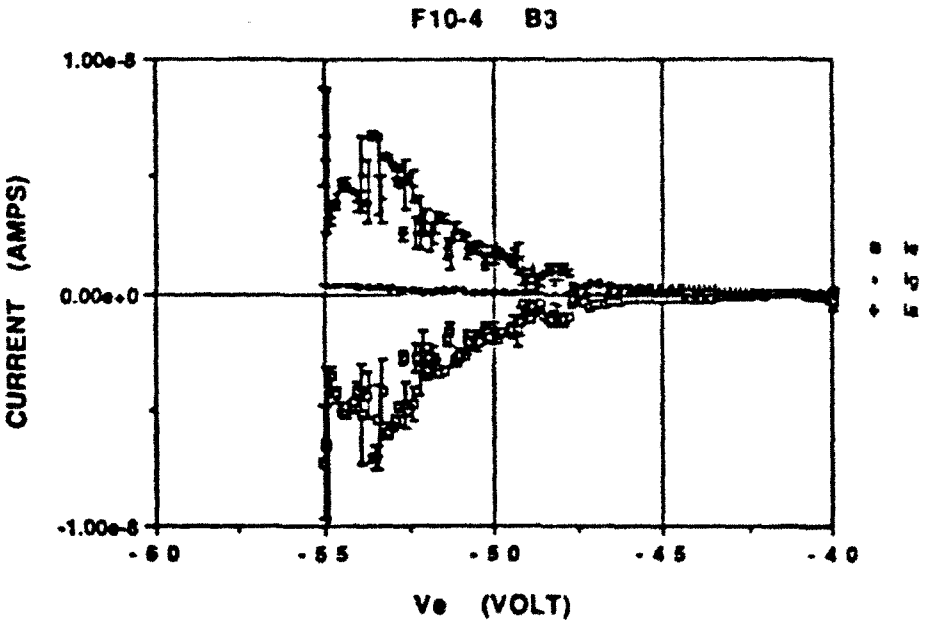


Figure 1 F10-4 B3 Shows high anode current relative to the gate current.

TABLE I SUMMARY OF TESTING RESULTS

ID	tip	diel	ditk kÅ	size u	Gtk kÅ	Base u	space u	num pts	Ig uA	Ia uA	Max V volt
9	Au	SiO	4	2.5	1	1.5	10	400		None	-136
9	Au	SiO	4	2.5	1	2.5	8	400	0.1	trace	-48
9	Au	SiO	4	2.5	1	2.5	8	400	0.01	trace	-24
9	Au	SiO	4	2.5	1	2.5	8	400	0.01	trace	-8
9	Au	SiO	4	2.5	1	2.0	8	400		None	-166
9	Au	SiO	4	2.5	1	2.0	8	400	0.1	None	-12
9	Au	SiO	4	2.5	1	2.0	8	400	0.1	None	-63
9	Au	SiO	4	2.5	1	2.0	8	400	0.1	None	-42
9	Au	SiO	4	2.5	1	2.0	5	10000	0.1	None	-26
10	Au	SiO	4	2.0	2	2.5	8	400		trace	-86
10	Au	SiO	4	2.0	2	2.5	8	400		None	-52
10	Au	SiO	4	2.0	2	1.5	3.54	3200		None	-93
10	Au	SiO	4	2.0	2	1.5	8	400		1 uA*	
10	Au	SiO	4	2.0	2	2.0	5	1600		trace	-55
10	Au	SiO	4	2.0	2	2.5	8	400	0.1	None	-69V
10	Au	SiO	4	2.0	2	2.5	8	400	0.1	None	
10	Au	SiO	4	2.0	2	2.5	8	400	0.1	None	-18
10	Au	SiO	4	2.0	2	2.5	8	400		trace	-50
10	Au	SiO	4	2.0	2	2.0	8	400	0.1	trace	-55
10	Au	SiO	4	2.0	2	2.0	8	400		0.7	
10	Au	SiO	4	2.0	2	2.0	8	400		trace	-55
10	Au	SiO	4	2.0	2	2.0	8	400	2.7uA	none	-74
10	Au	SiO	4	2.0	2	1.5	3.54	20000		none	-70
10	Au	SiO	4	2.0	2	1.5	3.54	20000		none	-95
10	Au	SiO	4	2.0	2	2.0	5	10000		none	-68
11	Au	SiN	6	1.5	1	2.5	8	400	1.0	none	-30
11	Au	SiN	6	1.5	1	2.5	8	400	0.1	none	-20
11	Au	SiN	6	1.5	1	2.5	8	400		none	
11	Au	SiN	6	1.5	1	2.0	8	400	0.1	none	-26
11	Au	SiN	6	1.5	1	2.0	8	400	0.1	none	-21
11	Au	SiN	6	1.5	1	2.0	8	400	Large		-60
11	Au	SiN	6	1.5	1	2.0	5	10000	0.1	none	-25
12	Au	SiN	6	1.0	2	2.5	8	400	0.1	none	-16
12	Au	SiN	6	1.0	2	2.5	8	400	0.1	none	-12
12	Au	SiN	6	1.0	2	1.5	10	400	0.1	none	-21
12	Au	SiN	6	1.0	2	1.5	8	400	0.1	none	-20
12	Au	SiN	6	1.0	2	1.5	8	400	0.1	none	-13
12	Au	SiN	6	1.0	2	2.0	5	1600	0.1	none	-10
12	Au	SiN	6	1.0	2	1.5	3.54	20000	0.1	none	-10

TABLE I (CONT) SUMMARY OF TESTING RESULTS

ID	tip	diel	ditk kÅ	size u	Gtk kÅ	Base u	space u	num pts	Ig uA	Is uA	Max V volt
13	Pt	SiO	6	1.5	2	2.5	8	400	1.1	.004	-54
13	Pt	SiO	6	1.5	2	1.5	10	400		trace	-63
13	Pt	SiO	6	1.5	2	1.5	10	400		1.0	-160
13	Pt	SiO	6	1.5	2	1.5	8	400	51	trace	-160
13	Pt	SiO	6	1.5	2	1.5	8	400	0.1	trace	-62
13	Pt	SiO	6	1.5	2	2.0	5	1600	0.3	none	-42
13	Pt	SiO	6	1.5	2	2.0	5	1600	0.45	none	-35
13	Pt	SiO	6	1.5	2	2.0	8	400	0.15	none	-27
13	Pt	SiO	6	1.5	2	2.0	8	400	0.1	none	-12
13	Pt	SiO	6	1.5	2	1.5	3.5	20000	1.0	none	-60
13	Pt	SiO	6	1.5	2	2.0	5	10000	0.15	none	-24
14	Pt	SiO	6	1.0	2	2.5	8	400	0.02	trace	-115
14	Pt	SiO	6	1.0	2	2.5	8	400	0.3	8**	
14	Pt	SiO	6	1.0	2	2.5	8	400	0.02	0.8	
14	Pt	SiO	6	1.0	2	2.5	8	400		none	-53
14	Pt	SiO	6	1.0	2	2.5	8	400	0.0005	0.001	-93
14	Pt	SiO	6	1.0	2	1.5	10	400	0.002	trace	-50
14	Pt	SiO	6	1.0	2	1.5	10	400	0.3	0.7	
14	Pt	SiO	6	1.0	2	1.5	8	400	0.02	0.60	-137
14	Pt	SiO	6	1.0	2	1.5	8	400	0.1	trace	-55
14	Pt	SiO	6	1.0	2	1.5	8	400	0.001	0.19	-116V
14	Pt	SiO	6	1.0	2	1.5	8	400	0.004	0.0012	-50V
14	Pt	SiO	6	1.0	2	1.5	8	400	8	none	-28
14	Pt	SiO	6	1.0	2	2.0	5	1600	0.5	trace	-115
14	Pt	SiO	6	1.0	2	2.0	5	1600	0.1	trace	-60
14	Pt	SiO	6	1.0	2	2.0	5	1600	0.1	trace	-117
14	Pt	SiO	6	1.0	2	2.0	5	1600	0.13	trace	-100
14	Pt	SiO	6	1.0	2	2.0	8	400	0.1	none	-28
14	Pt	SiO	6	1.0	2	2.0	8	400		none	-50
14	Pt	SiO	6	1.0	2	2.0	8	400	0.04	0.6***	-75
14	Pt	SiO	6	1.0	2	1.5	3.5	20000	0.1	none	-21
14	Pt	SiO	6	1.0	2	1.5	3.5	20000		trace	-121
14	Pt	SiO	6	1.0	2	1.5	3.5	20000		0.5	-50
14	Pt	SiO	6	1.0	2	1.5	3.5	20000	1	trace	-85
14	Pt	SiO	6	1.0	2	2.0	5	10000	0.5	trace	-105
14	Pt	SiO	6	1.0	2	2.0	5	10000	0.15	trace	-50
14	Pt	SiO	6	1.0	2	2.0	5	10000	0.09	trace	-62
14	Pt	SiO	6	1.0	2	2.0	5	10000		trace	-82

* First device to show emission.
** Spiked then failed.
*** Produced substaintial brightness on phospher but had a poor image.

The one to one correspondence between the emitter current and the anode current is clearly seen in figure 2. Even the time variations (represented by the standard deviation of the ten measurements per data point) are clearly seen when the standard deviation is plotted as error bars for both currents simultaneously. Figure 3 is yet another device where the anode current is high with respect to the gate current. In figure 3 the three currents are plotted verses the time of the measurement. The plateau in the three currents occurs during a hold period when the voltage is not changed.

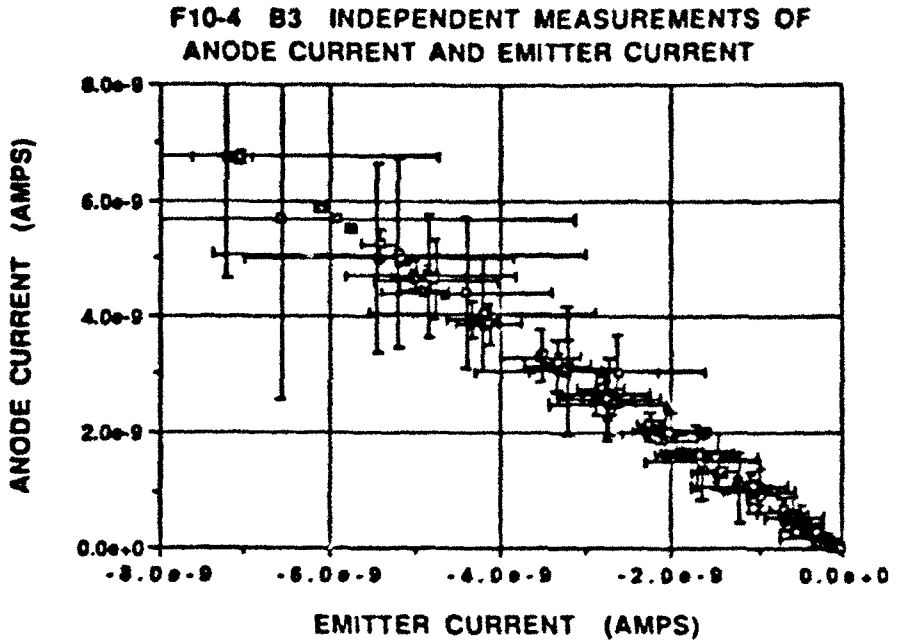


Figure 2 One to one correspondence between the anode current and the emitter current.

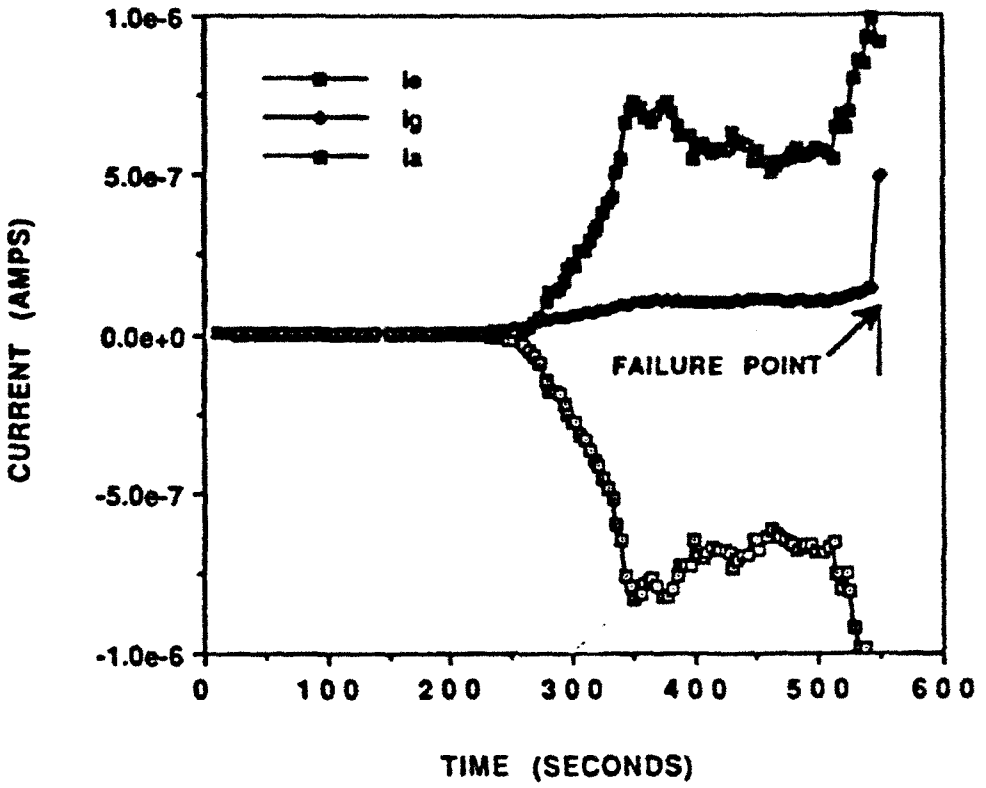


Figure 3 F13-8 B2 Shows high anode current relative to the gate current as a function of time of the measurement. The plateau in the currents is where the gate to emitter voltage is held fixed.

From time to time samples are aged over night, by leaving then on the measurement system at a constant DC voltage. In most cases these devices are found to be failed the next morning. Figure 4 is an example of almost 20 hours of aging on the measurement station. The device failed at about 17 hours. Numerous attempts have been made to slowly age a new emitter, the results have been mixed.

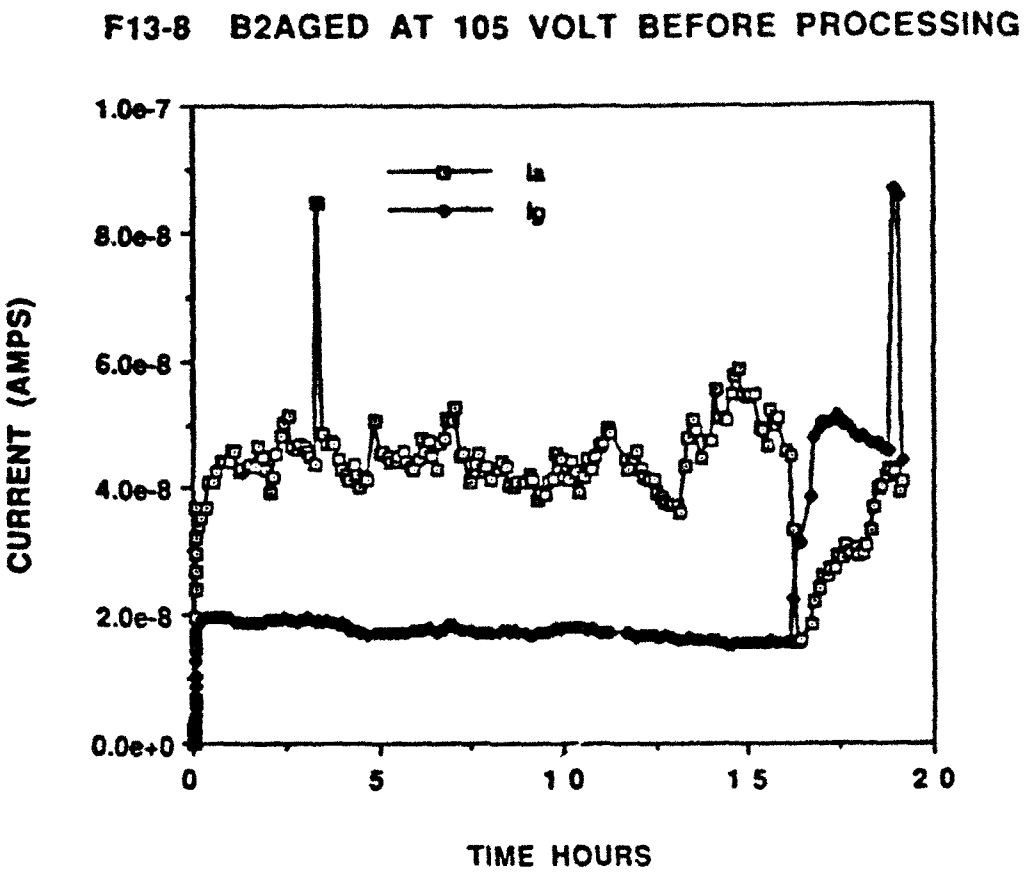


Figure 4 F13-8 B2 is a overnight age at constant DC voltage.

Several of the devices that show high emission current relative to the leakage current are plotted on a Fowler-Nordheim curve in figure 5. Clearly, the field emission behavior is evidenced over more the five orders of magnitude. From these Fowler-Nordheim plots the transconductance can be determined. The transconductance gm ranges from .03 uS for F13-8 B2 to 3.2 uS for F19-3 D3.

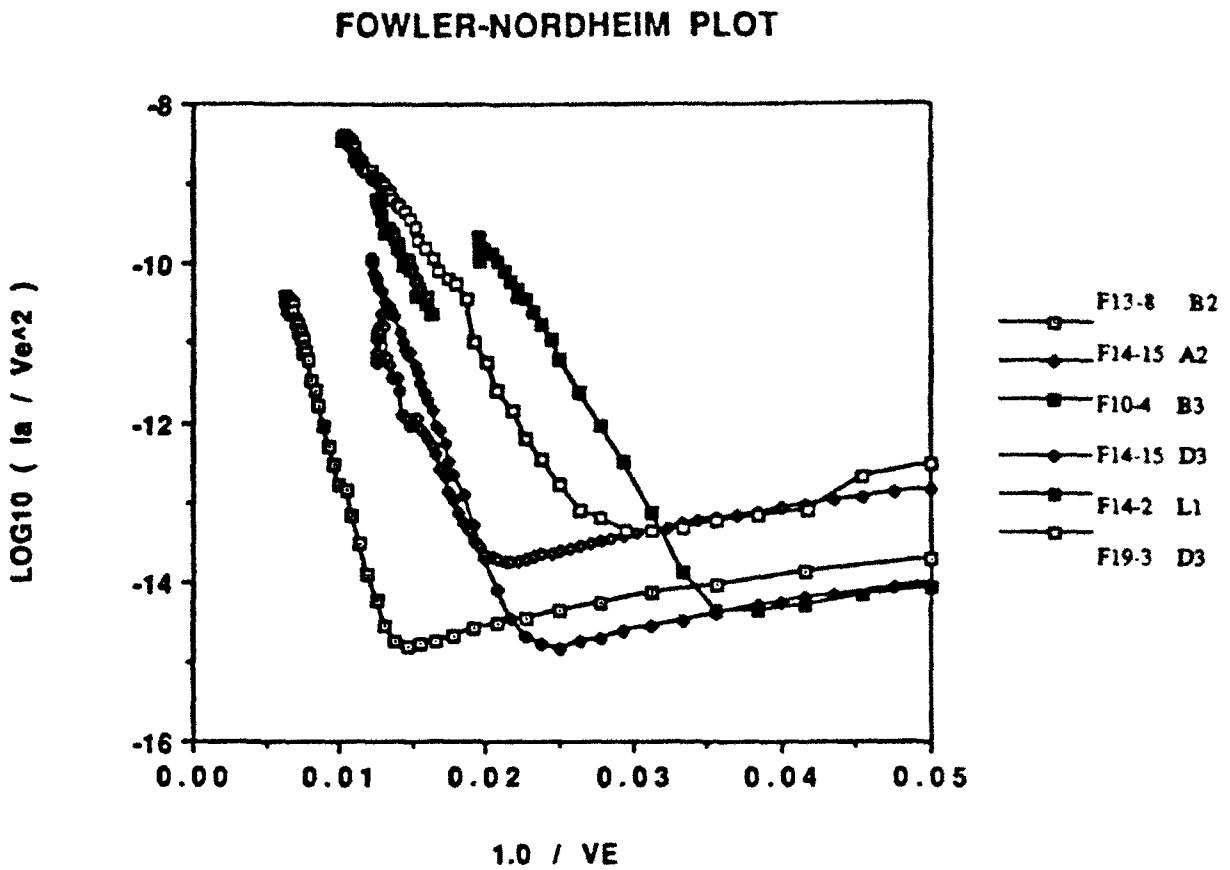


Figure 5 Fowler-Nordheim curve for several of the best emitters.

Several techniques have been explored in an attempt to improve the device performance by post fabrication processing. We have built into the measurement system a plasma cleaning capability and have explored various plasmas in an attempt to affect performance. Figure 6 shows the results of sequential oxygen and hydrogen plasma cleanings. This process does have an affect on the leakage and the anode currents. Typically after an oxygen plasma cleaning the anode current is reduced and in some cases eliminated completely from what it was before the cleaning. The leakage current is sometime reduced and sometime increased but in both cases the voltage that can be impressed between the gate to emitter increases. When the oxygen plasma cleaning is followed by a hydrogen plasma cleaning , as is the case in figure 6, the emission returns as does the leakage. It appears the by adjusting the power and time of each of the plasma steps an improved condition can be obtained.

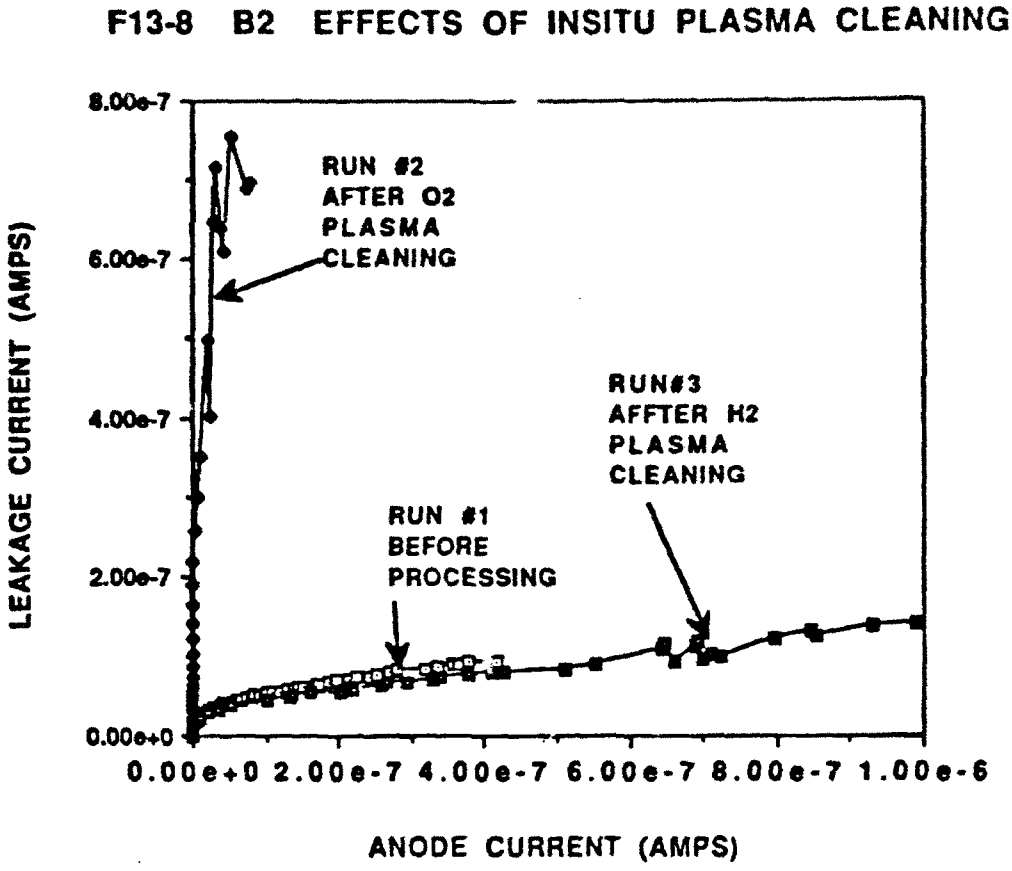


Figure 6 Demonstrates the effect of oxygen and hydrogen plasma cleaning. The oxygen plasma cleaning was done first followed by the hydrogen plasma cleaning.

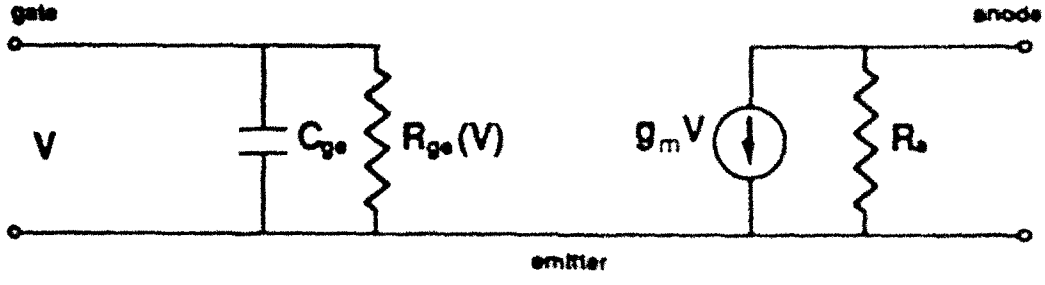
3.0 LOW WORK FUNCTION MATERIAL

3.1 IDENTIFY CANDIDATE MATERIALS

In addition to the low work function materials identified in quarterly progress report #2 an attempts to alter the tip work function insitu is being setup for the next run and will be reported in the next quarter. In the experiment a barium source will be mounted below the hollow tube anode so that a stream of barium can be directed to the emitter during operation. We will be looking for changes in the emission (anode) current when the stream of barium is turned on.

4.0 FEA Equivalent Model

A preliminary equivalent circuit model for the FEA has been generated and is shown below. This is a bare-bones equivalent circuit including only the first order effects we have observed. There is one important feature that has been observed in recent FEA testing and that is the gate voltage dependent resistance. This component is expected if some gate interception of emitter current exists. We have seen this distinctly on several samples and seen no evidence of it on several other samples. Although we suspect that geometries in which the emitter tip is recessed below the plane of the gate would enhance gate interception, we have not seen incontrovertible evidence that geometrical factors are key to this phenomenon.



Equivalent circuit of FEA including gate interception.

Capacitance per tip ranges from a low of 0.9 fF/tip for a 20,000 tip array with 3.5μm tip spacing and a 6000 Å SiO_2 dielectric to a high of 20 fF/tip for a 400 tip array with 10μm spacing and a 4000 Å Si_3N_4 dielectric. Measurement data from sample 13-8 B2 gives the following current voltage characteristic:

$$I = AV^2 e^{\frac{-B}{V}} = 6.63 \times 10^{-7} V^2 e^{\frac{-650}{V}}$$

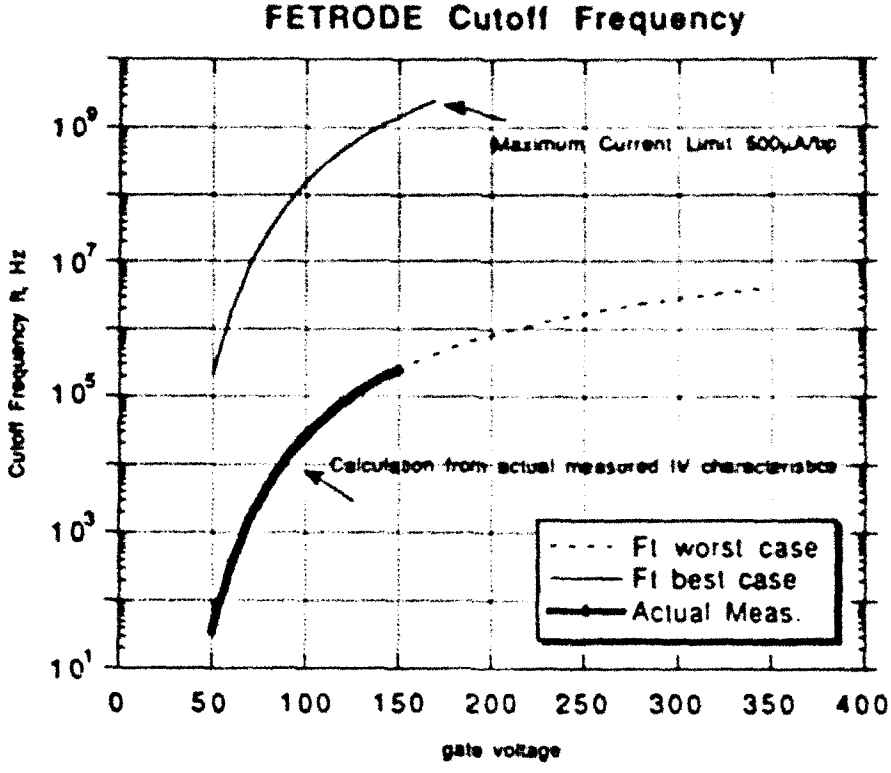
The above characteristic was obtained from measured data up to a maximum gate potential of 150V. The sensitivity of our measurement system is such that five orders of magnitude of I/V^2 were obtained for this particular device from the onset of emission to burnout. Several unknown factors about the measured data make it difficult to obtain an accurate prediction of cutoff frequency, however, we can determine the best and worst case cutoff frequencies as follows:

1) Measured data represents emission from at least one and at most 400 tips. If uniform emission was obtained from all 400 tips then actual measured transconductance divided by array capacitance gives the cutoff frequency. The array capacitance was about 5 pF.

2) If only a single tip was responsible for the entire emission current, then the appropriate capacitance is that for a single tip (about 0.9 fF).

These considerations were used to generate the plot shown below. The actual cutoff frequency of the device under test reached a maximum calculated value of 20 kHz. If single tip emission was responsible and if through the proper aging procedure or other treatment all other tips in the array could be "turned on" to the same emission level, then the best case cutoff frequency would result, about 2 GHz. Note that the "best case" curve

stops at a current level of 500 μA/tip, a rough maximum current level obtained by Spindt and others.



As we can see from the plot above, the cutoff frequency is only likely to be about 1GHz with the existing materials and geometries. To significantly enhance frequency performance a material change in the tip is needed. Key to determining the actual cutoff frequency of the FETRODE device is the ability to deduce the number of tips that participate in emission. To this end we have planned to conduct several experiments using our electron emission microscope.